Amendments to the Claims:

1. (Currently Amended) A processor comprising:

a cache having a plurality of hit lines; and

a selector to provide a data during a clock cycle from a plurality of memory locations associated with the plurality of hit lines in the cache;

a multi-hit detection circuit coupled to the hit lines to detect multiple hits in the cache during the clock cycle based on hit signals on the hit lines, ~~and~~ the multi-hit detection circuit comprising a NAND gate with transistor pairs; and

~~to generate an error flag generated during a clock cycle to indicate if multiple hits have occurred, and to provide a data from the cache during the clock cycle.~~

an error flag generated by an inverter output in the multi-hit detection circuit during the clock cycle to indicate multiple cache hits.

2. (Original) The processor of claim 1, wherein the cache includes a plurality of comparators coupled to the hit lines to generate the hit signals based on comparisons between cache tags and a lookup tag.

3. (Original) The processor of claim 2, wherein the selector includes a multiplexer coupled to the hit lines to select data based on the hit signals.

4. Cancelled.

5. (Original) The processor of claim 1, wherein the detection circuit includes a NAND gate having pull-down transistor pairs coupled to the hit lines to pull an output node of the NAND gate low if two different hit signals indicate a hit.

6. (Original) The processor of claim 5, wherein the inverter is coupled to the output node to generate the error flag.

7. (Original) The processor of claim 5, wherein the cache is a multi-way set associative cache.

Claims 8-12 (Cancelled).

13. (Currently Amended) A method of detecting multi-hit errors in a cache, the method comprising:

comparing a plurality of cache tags stored in each of a plurality of ways associated with a indexed set to a lookup tag to generate a plurality of hit signals during a clock cycle;

selecting selected data from a plurality of memory locations associated with the indexed set based~~, at least in part,~~ on the plurality of hit signals during the clock cycle; ~~and~~

comparing pairs of the plurality of hit signals during the clock cycle using a NAND gate with transistor pairs to determine if any two hit signals both indicate a hit;

generating an error flag using an inverter output during ~~a~~ the clock cycle indicating the validity of the selected data ~~by comparing pairs of the plurality of hit signals to determine if any two hit signals both indicate a hit and providing a data from the cache~~.

14. (Currently Amended) The method of claim ~~10~~ 13, wherein comparing the plurality of cache tags includes comparing four cache tags of a four-way set associative cache to the lookup tag to generate four hit signals.

15. (Original) The method of claim 14, wherein generating the error flag includes providing all pairings of the plurality of hit signals to gates of series-coupled pull-down transistor pairs of a NAND gate.

16. (Original) The method of claim 13, wherein generating the error flag includes providing pairings of the plurality of hit signals to gates of series-coupled pull-down transistor pairs of a NAND gate.

17. (Original) The method of claim 16, wherein generating the error flag further includes inverting an output of the NAND gate.